Single Channel, Ultra-Low Resistance Load Switch

Check for Samples: TPS22965

FEATURES

- **Integrated Single Channel Load Switch**
- **Input Voltage Range: 0.8V to 5.5V**
- **Ultra low R_{ON} Resistance**
  - **R_{ON} = 18mΩ at V_{IN} = 5V (V_{BIAS} = 5V)**
  - **R_{ON} = 18mΩ at V_{IN} = 3.6V (V_{BIAS} = 5V)**
  - **R_{ON} = 18mΩ at V_{IN} = 1.8V (V_{BIAS} = 5V)**
- **6A Maximum Continuous Switch Current**
- **Low Quiescent Current (50µA)**
- **Low Control Input Threshold Enables Use of 1.2-V/1.8-V/2.5-V/3.3-V Logic**
- **Configurable Rise Time**
- **Quick Output Discharge (QOD)**
- **SON 8-pin Package With Thermal Pad**
- **ESD Performance Tested per JESD 22**
  - **2KV HBM and 1KV CDM**

APPLICATIONS

- **Ultrabook™**
- **Notebooks/Netbooks**
- **Tablet PC**
- **Consumer Electronics**
- **Set-top Boxes/Residental Gateways**
- **Telecom Systems**
- **Solid State Drives (SSD)**

DESCRIPTION

The TPS22965 is a small, ultra-low R_{ON}, single channel load switch with controlled turn on. The device contains a N-channel MOSFET that can operate over an input voltage range of 0.8V to 5.5V and can support a maximum continuous current of 6A. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. In TPS22965, a 220-Ω on-chip load resistor is added for quick output discharge when switch is turned off.

The TPS22965 is available in a small, space-saving 2mm x 2mm 8-SON package (DSG) with integrated thermal pad allowing for high power dissipation. The device is characterized for operation over the free-air temperature range of –40°C to 85°C.

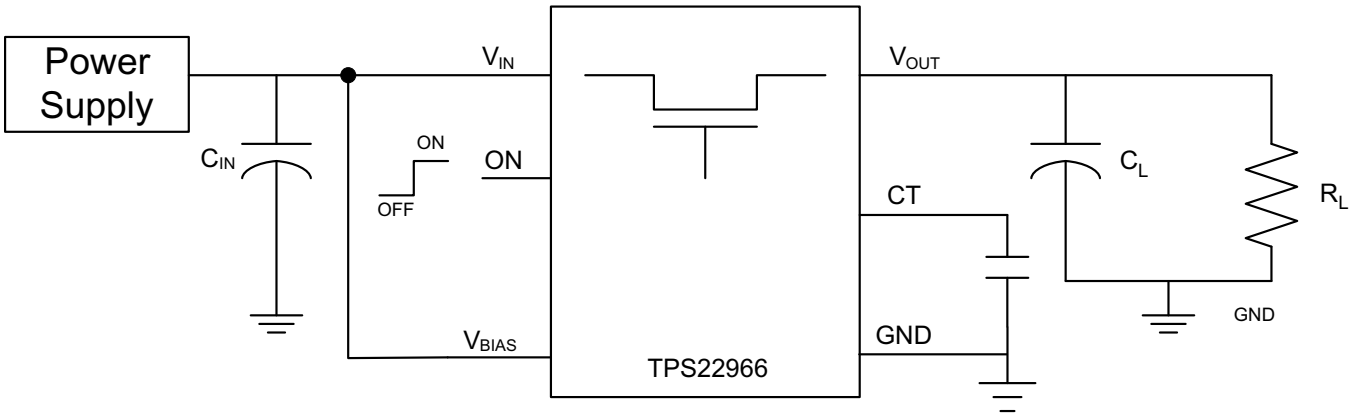
Feature List

R_{ON} Typical at 3.6 V (V_{BIAS} = 5V)	18 mΩ
Rise Time(1)	Adjustable
Quick Output Discharge(2)	Yes
Maximum Output Current	6 A
GPIO Enable	Active High
Operating Temperature	–40°C to 85°C

(1) See Application Information section for CT value vs. rise time.

(2) This feature discharges output of the switch to GND through a 220-Ω resistor, preventing the output from floating.

PRODUCT PREVIEW



Typical Application

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Ultrabook is a trademark of Intel.

PACKAGING INFORMATION

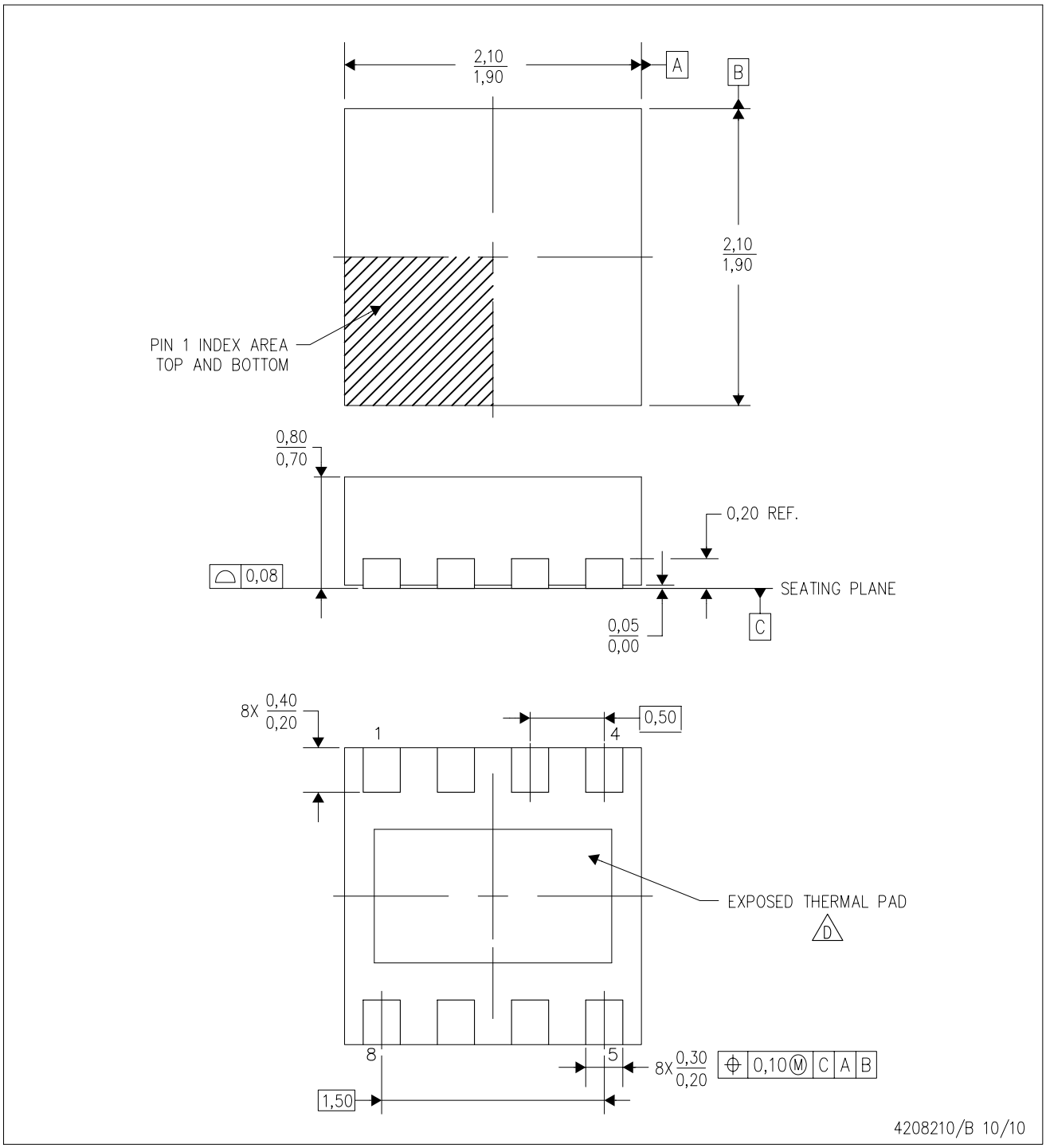
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS22965DSGR	PREVIEW	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS22965DSGT	PREVIEW	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–229.

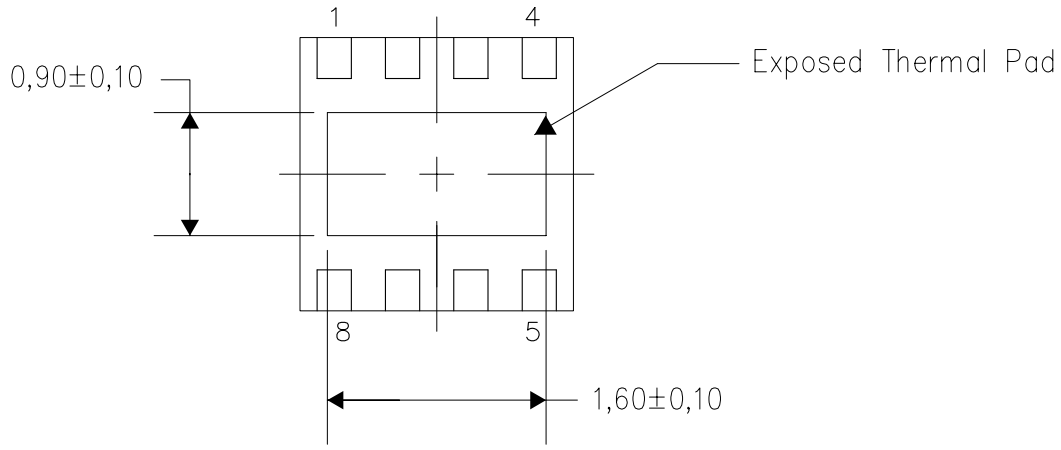
DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



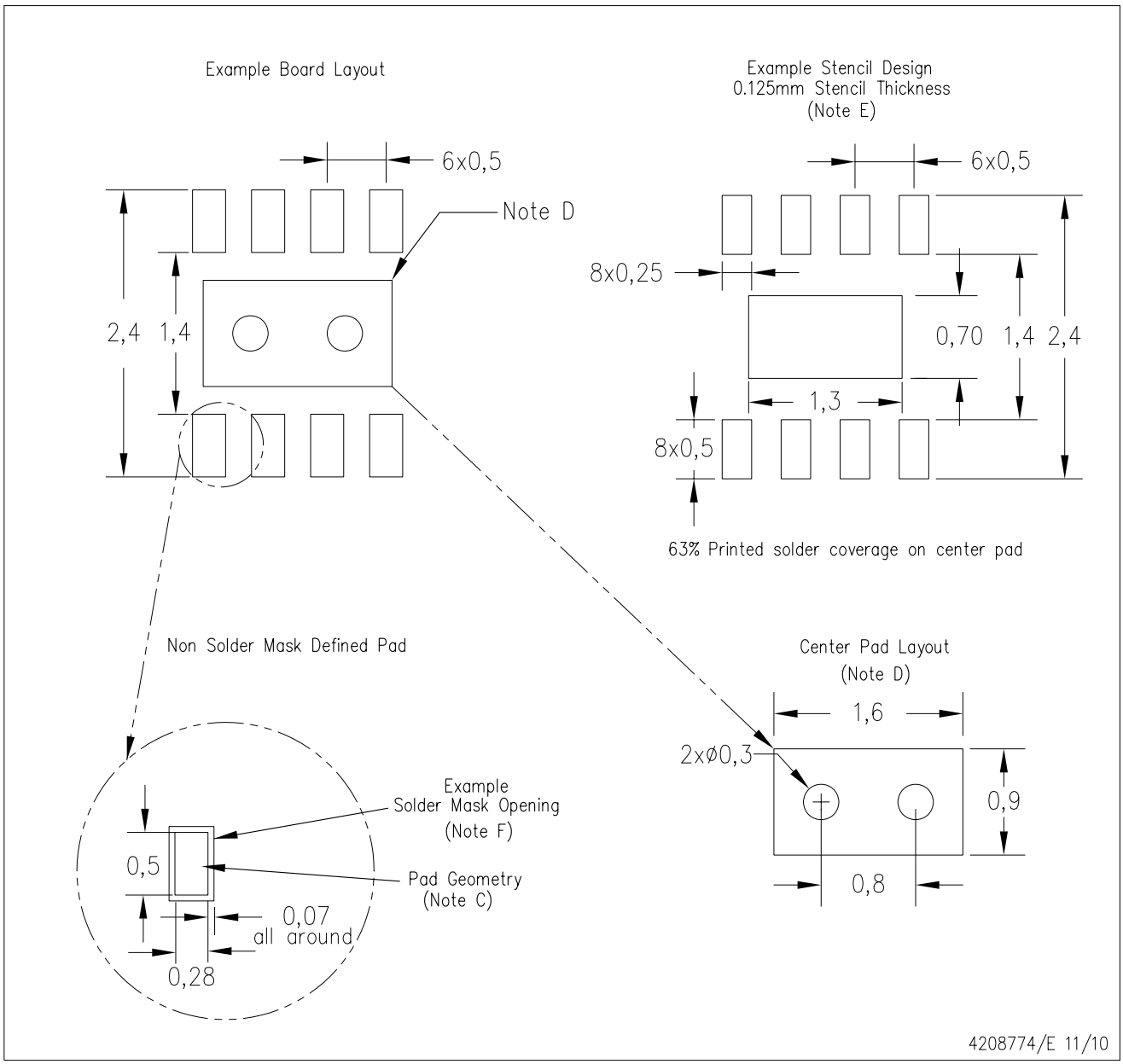
Bottom View

Exposed Thermal Pad Dimensions

4208347/E 11/10

NOTE: A. All linear dimensions are in millimeters

DSG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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